Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims

Claims 1-2 (canceled)

Claim 3 (currently amended): ~~The memory device according to claim 2~~ A memory device comprising:

a memory cell array having a plurality of memory cells, first and second bitlines, and first and second wordlines, each of said memory cells being coupled to one of said first bitlines, one of said second bitlines, one of said first wordlines and one of said second wordlines;

a first wordline decoder being coupled to said multitude of first wordlines to activate one of said wordlines;

a second wordline decoder being coupled to said multitude of wordlines to activate one of said second wordlines;

wherein each of said first and second wordline decoders is designed to perform an access to one of said memory cells by enabling one of the multitude of said wordlines;

a refresh control circuit arrangement including a contention circuit that allocates a refresh to one of said wordline decoders, whereby said one of said wordline decoders is currently not used for an external access to one of the memory cells of said memory cell array; and

wherein said contention circuit is designed to select said one of said first and second wordline decoders to perform a refresh operation to said memory cells connected to said multitude of wordlines coupled to said one of said first and second wordline decoders and is designed to select another one of said first and second wordline decoders to perform an external access and to issue a wait cycle for said one of said first and second decoders when said one wordline decoder receives an external request for an access.

Claim 4 (currently amended): ~~The memory device according to claim 1~~ A memory device comprising:

a memory cell array having a plurality of memory cells, first and second bitlines, and first and second wordlines, each of said memory cells being coupled to one of said first bitlines, one of said second bitlines, one of said first wordlines and one of said second wordlines;

a first wordline decoder being coupled to said multitude of first wordlines to activate one of said wordlines;

a second wordline decoder being coupled to said multitude of wordlines to activate one of said second wordlines;

a refresh control circuit arrangement including a contention circuit that allocates a refresh to one of said wordline decoders, whereby said one of said wordline decoders is currently not used for an external access to one of the memory cells of said memory cell array; and

wherein said refresh control circuit arrangement comprises a refresh address counter that counts the addresses of the wordlines to be refreshed and comprises a comparator to compare said address of said wordline to be refresh with an address of a wordline to be accessed upon an external request, wherein in response to an address match a refresh cycle is suppressed.

Claim 5 (canceled)

Claim 6 (currently amended): ~~The memory device according to claim 5~~ A memory device comprising:

a memory cell array having a plurality of memory cells, first and second bitlines, and first and second wordlines, each of said memory cells being coupled to one of said first bitlines, one of said second bitlines, one of said first wordlines and one of said second wordlines;

a first wordline decoder being coupled to said multitude of first wordlines to activate one of said wordlines;

a second wordline decoder being coupled to said multitude of wordlines to activate one of said second wordlines;

a first access port and a second access port, said first access port comprising said first wordline decoder and said second access port comprising said second wordline decoder;

a first terminal to provide a first select signal to enable an access through said first port;

a second terminal to provide a second port select signal to enable an access through said second port;

a refresh control circuit arrangement including a contention circuit that allocates a refresh to one of said wordline decoders, whereby said one of said wordline decoders is currently not used for an external access to one of the memory cells of said memory cell array; and

said contention circuit providing an address of a wordline of which the memory cells are to be refreshed to said row decoder of said first access port, if either a) the port select signal provided to said first access port is activated and the port select signal provided to said second access port is deactivated or b) ~~wherein said contention circuit provides an address of a wordline of which the memory cells are to be refreshed to said row decoder of said first access port, if~~ the port select signals provided to said first and second access ports are both activated, and wherein said contention circuit issues a wait signal to delay an externally requested access to a memory cell through said first access port during said refresh performed through said first access port.

Claim 7 (currently amended): The memory device according to claim ~~5~~ 3, 4 or 6 wherein said contention circuit is designed to perform a wait cycle for an externally requested access for one of said ports, if the first and the second port select signals are activated.

Claim 8 (currently amended): The memory device according to ~~any of claims 1 to 7,~~ claim 3, 4, or 6 wherein the memory cells each comprise a storage device having a first and a second terminal, a first access transistor connected to said first terminal and a second access transistor connected to said second terminal, said first access transistor connected to one of the multitude of said first wordlines and first bitlines, said second access transistor connected to one of the multitude of second wordlines and second bitlines.

Claims 9-10 (canceled)

Claim 11 (currently amended): ~~The method according to claim~~ A method of operating a memory device wherein said memory device has first and second access ports, memory cells being arranged in a multitude of rows, each row being accessible through said first and said second ports, and first and second row decoders, the method comprising:

decoding one of said rows in response to a respective row address, wherein a refresh is performed on the memory cells of one of said rows by enabling said row through the first row decoder while another row is accessed in response to an externally requested access through the second row decoder; and

~~further comprising the step of~~ counting the row address of rows to be refreshed and suppressing a refresh of the memory cells of a row when a row address of an externally requested access and the row address of said row to be refreshed match each other.

Claim 12 (new): The memory device according claim 7 wherein the memory cells each comprise a storage device having a first and a second terminal, a first access transistor connected to said first terminal and a second access transistor connected to said second terminal, said first access transistor connected to one of the multitude of said first wordlines and first bitlines, said second access transistor connected to one of the multitude of second wordlines and second bitlines.

Claim 13 (new): A memory array comprising:

a plurality of memory cells arranged in a plurality of rows and columns, wherein a memory cell of the array comprises first and second wordlines in a row direction and first and second bitlines in a column direction;

first and second ports capable of performing memory access and refresh operations, the first wordlines and bitlines corresponding to the first access port and the second wordlines and bitlines corresponding to the second access ports; and

a refresh control circuit for controlling refresh operations, the refresh control circuit, when a refresh operation is requested, allocates the requested refresh operation to either the first or second port, whichever is not occupied with a memory access operation to reduce contention between the refresh operation and memory access operation.

Claim 14 (new): The memory array of claim 13 wherein the refresh control circuit comprises normal and power down operating modes.

Claim 15 (new): The memory array of claim 13 or 14 wherein the refresh control circuit allocates the refresh operation

to either the first or second port if neither of the ports is occupied with a memory access operation;

to the second port if the first port is occupied with a memory access operation;

to the first port if the second port is occupied with a memory access operation; or

when both first and second ports are occupied with respective memory access, delays the memory access to one of the first or second ports to enable refresh operation to the one of the first or second ports while allowing the memory access operation to continue at the other of the first or second port.

Claim 16 (new): The memory array of claim 15 wherein the refresh control circuit rotates priority of access between the first and second ports when contention between refresh and memory access operations occurs.

Claim 17 (new): The memory array of claim 13 or 14 wherein the refresh control circuit refreshes the memory cells one row at a time within a refresh cycle, wherein a row can be refreshed either via the first or second port.

Claim 18 (new): The memory array of claim 17 wherein the refresh control circuit disables the refresh operation if the memory access is a read memory access and row addresses of the refresh and memory access operations are the same.

Claim 19 (new): The memory array of claim 17 wherein the refresh control circuit disables the refresh operation if the memory access is a write memory access and row addresses of the refresh and memory access operations are the same, the memory cell of the row accessed is written to while other cells of the row accessed are read from.

Claim 20 (new): The memory array of claim 17 wherein the refresh control circuit allocates the refresh operation of a row:

to either the first or second port if neither of the ports is occupied with a memory access operation;

to the second port if the first port is occupied with a memory access operation if a refresh row address is different from a row address of the memory access operation;

to the first port if the second port is occupied with a memory access operation if the refresh row address is different from the memory row address; or

when both first and second ports are occupied with respective memory accesses, delays the memory access to one of the first or second ports to enable refresh operation to the one of the first or second ports while allowing the memory access operation to continue at the other of the first or second port if the refresh row address is different from the row address.

Claim 21 (new): The memory array of claim 20 wherein the refresh control circuit disables the refresh operation if the memory access is a read memory access and row addresses of the refresh and memory access operations are the same.

Claim 22 (new): The memory array of claim 20 wherein the refresh control circuit disables the refresh operation if the memory access is a write memory access and row addresses of the refresh and memory access operations are the same, the memory cell of the row accessed is written to while other cells of the row accessed are read from.

Claim 23 (new): The memory array of claim 20 wherein the refresh control circuit rotates priority of access between the first and second ports when contention between refresh and memory access operations occurs.

Claim 24 (new): The memory array of claim 23 wherein the refresh control circuit disables the refresh operation if the memory access is a read memory access and row addresses of the refresh and memory access operations are the same.

Claim 25 (new): The memory array of claim 23 wherein the refresh control circuit disables the refresh operation if the memory access is a write memory access and row

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addresses of the refresh and memory access operations are the same, the memory cell of the row accessed is written to while other cells of the row accessed are read from.